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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WONG, LINDA	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,198	BREWER, SYMON	
	Examiner	Art Unit	
	Linda Wong	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments filed 2/2/2006 have been fully considered but the arguments regarding the drawings, claims 1-20 are not persuasive.
2. On pages 6-8, the applicant argues additional written labels are not necessary to understand the drawings. The examiner feels the drawings with only a cloud, arrows and multiple boxes do not describe the components of the drawings. Thus, the examiner is requiring the applicant to submit corrections to the drawings to include written labels that describe the components in the invention.
3. On page 6, the applicant argues the examiner gave no further explanation as to why the drawings are objected. The examiner stated in the office action mailed 10/5/2005 that the drawings require written labels to clarify the drawings, which explicitly indicates the drawings are defective because there are no written labels to describe the components in the invention which are shown in the drawings.
4. On page 6, the applicant argues the drawings contain "universal symbols for modules, circuits, and components". The applicant gives an example referring to Fig. 1. The applicant argues the symbol "cloud" is a universal symbol for "network". Without the written description from the specification, a "cloud" can be a symbol for multiple components. Furthermore, the drawings show only boxes or squares with a numerical label. A box or square, without a written label, does not describe to one of ordinary skilled in the art any aspect of the invention. Since these drawings a published, one of ordinary skill in the art must be able to understand the drawings and comprehend the invention through the drawings. Although one can say a box

or a square is a "universal symbol", without written labels, one of ordinary skill in the art can understand that the "universal symbol" as a square or box or a cloud and cannot understand the components of the invention without a written label.

5. On page 7, the applicant argues the examiner's rejection is inconsistent with the requirements expressly set forth under 37 CFR 1.74. The examiner would like to point out the requirements for the drawings as indicated in 37 CFR 1.83, which states "The drawings in a US application must show every feature of the invention specified in the claims. However, conventional features disclosed in the description and claims, where their detailed illustration is not essential for a proper understanding of the invention, should be illustrated in the drawing in the form of graphical drawing symbol or a labeled representation (e.g. a labeled rectangular box). ..." Figures 1-3 show multiple rectangular boxes which does not describe the invention nor the components in the invention. Thus, written labels are necessary for understanding the drawing.

6. On page 8, the applicant argues "the USPTO is a PCT receiving office and is bound by PCT Rule 11.11, which states that "... drawings shall not contain text matter, except a single word or words, when absolutely indispensable...". First, the applicant has submitted a US application, not a PCT application. The applicant is correct in stating the PCT rules, but such rules apply to PCT applications. Thus, for a US application, the written labels to the drawings are required. Second, the examiner has already stated that the drawings cannot be understood without written labels as stated in the previous office action objection where the drawings submitted

need further clarification to describe the invention. Since, the components shown as boxes in the drawings are essential to the applicant's invention, otherwise the claimed language would not include the components in the drawings, written labels accompanying the components of the drawings are necessary.

7. Regarding the objection to the drawings, please review the rejection as stated below for the additional clarification.

8. Regarding claim 1, on page 9, the applicant argues Kelkar fails to disclose a data signal. The examiner agrees but Kelkar discloses a reference, Ferraiolo et al, (Col. 2, lines 1-11 and Col. 1, lines 64-67), wherein Ferraiolo et al discloses measuring "data timing jitter within a digital communication link for monitoring digitally transmitted signals at a receiving point". (Col. 1, lines 64-67 and Col. 2, lines 1-12) It would be obvious to one skilled in the art to replace the clock signal to a data signal based on designer's choice and to eliminate jitter from the received data so to effectively determine the transmitted data. Please regard the new rejection to claim 1 as per the amended claim.

9. Regarding claim 1, on page 11, the applicant argues "Kelkar does not teach or suggest digitally latching and converting." The examiner respectfully disagrees. Col. 4, lines 25-67 and Col. 5, lines 1-2, Kelkar discloses "In the preferred embodiment, the four bit word 28 indicates the amount of jitter between the rising edge of the reference and measured clocks." In order to measure a 4 bit word, the system would must be a digital system. Kelkar further discloses "In Fig. 3, the reference signal 22, along with the four delay clocks 36,38,40,42, create five

possible time slices N1-N5 (ie., 46,48,50,52, and 54) in which the rising transition edge of the measured clock signal falls in N1, edge sorting circuit would output a 0000 since the jitter is less than 100 picoseconds." By outputting "0000", the edge sorting circuit inherently functions as a digital edge sorting circuit, since it outputs a digital word. Also, Kelkar discloses, in Fig. 3, the outputs of the delayed clocks. The clocks shown are pulsing signals fluctuating from 0 to 1, which indicates the delay line outputs a digital signal. Although the applicant argues that Kelkar discloses an analog system due to the enclosed capacitor in the loop filter, digital capacitors are well known in the art. Since Kelkar discloses outputs from the delay line are digital signals and the delay line is controlled by the capacitor, the capacitor would be a digital capacitor. (Fig. 3, Fig. 5)

10. Regarding claims 1, on page 11, the applicant argues the calibration system disclosed by Kelkar in Fig. 5 is unnecessary to measure jitter. Col. 6, lines 28-35, Kelkar discloses "By using the calibration system, the total delay is automatically adjusted to the desired amount. Process variations as well as environmental differences in temperature and power supply voltage can be automatically tuned out using this calibration circuit. The result of using the calibration circuit and the adjustable delay inverters is that accurate time slices can be created for use by the latches in the sorting circuit of Fig. 2." Col. 3, lines 35-38, Kelkar discloses the purpose of the sorting circuit which is where the PLL disclosed in Fig. 5 is located as per the quotation above. "The main function of the edge sorting circuit 12 is to help measure the jitter defined as the delay between the transition edge of the

reference clock signal and the measured clock signal." Thus, Kelkar discloses detecting jitter and why PLL and edge sorting circuit is important. Furthermore, Kelkar discloses detecting the transition locations or time slices or time delay (Col. 3, lines 38-54 and Col. 4, lines 25-53) by using the PLL as disclosed in Fig. 5.

11. Regarding claims 1, on page 11, the applicant argues the combination of Kelkar and Yanagisawa et al has no motivation since no motivation has been cited or presented in either Kelkar or Yanagisawa et al. The examiner respectfully disagrees. Kelkar discloses a digital jitter measuring system comprising a edge sorting circuit comprising a PLL (Col. 3, lines 55-61 and lines 19-30), which "measure[s] transition edge", (Col. 3, lines 35-41) coupled to charge pump (Fig. 5, label 90) and a counter (Fig. 1, label 16). Yanagisawa et al discloses an edge detector detecting the transmission of the edges (Col. 8, lines 44-56) coupled to charge pump and a counter (Fig. 11, labels 107,2041 and 105). Due to the multiple of common components found in both Yanagisawa et al and Kelkar's invention, the references specifically hint to a possible combination.

12. Regarding claim 1, on page 12, the applicant argues one of ordinary skill in the art would not, even in hindsight, look to Kelkar for teachings relevant to the present invention since Kelkar's invention would only measure the jitter probability density function of a filtered jitter signal. Kelkar does not teach that the inputted signal is or is not filtered prior to being inputted into Kelkar's jitter measuring system, which indicates that filtering can be done prior to Kelkar's jitter measuring system. Furthermore the applicant does not claim a communications system but "A method

for measuring jitter on a data signal comprising ..." as recited in claims 1 and 6 and "Apparatus for measuring jitter on a data signal comprising ..." as recited in claims 11 and16. Thus, applicant's argument has not relevance to the claimed language due to the broadness of the independent claims.

13. Regarding claim 1, on page 12, the applicant argues the examiner does not show or cite a specific section in Kelkar to support the combination of Kelkar and Yanagisawa. The examiner respectfully disagrees, but the examiner has included in the prior art rejection below further explanation and clarity of the motivation for combination. Please refer to the rejection below.

14. Regarding claims 1, on page 14, the applicant argues Yanagisawa discloses an analog circuitry. The examiner respectfully disagrees. Yanagisawa et al discloses "A jitter detector obtains a phase different between input signals as a digital value to make jitter between signals easily detectable." (Abstract, line 1-3) Yanagisawa et al also discloses, in Fig. 8, digital signals inputted in to the edge detector (Fig. 7, labels 101,102,107 and fig. 8, labels 101,102), wherein the edge detector outputs a digital signal (Fig. 8, labels 1011,1021 and Fig. 7, labels 107,1011,1021). Yanagisawa et al also disclosed "Another object of the present invention is to provide a jitter detector and jitter detecting method that can detect jitter between input signals much more easily by utilizing the digital value and without increasing the circuit size thereof."

15. Regarding claim 1, on page 15, the applicant argues the applicant's invention gives jitter measurement on **every** transition of the input to be measured. Claim 1 does

not include such a recitation. The claim recites digitally generating data signal transitions locations but does not state that every transition of the data signal is measured.

16. Regarding claim 1, on page 15, the applicant argues the applicant's invention is purely digital and does not require a capacitor. The claims do not recite such a limitation thus, the references can use a capacitor to perform the functionality. The claim is interpreted in the broadest send of the claimed language and since such limitation is not recited, the applicant's argument not relevant.
17. Regarding claim 1, on page 15, the applicant argues the applicant's invention does not require a comparator. Yanagisawa uses a comparator to ensures the edge position is within limits or range, which reads on the limitation "edge position output to determine edge position movement in excess of a predetermined magnitude" as recited in claim 4. The applicant does not recite the limitation of not using a comparator, and since the reference reads on the limitation, the rejection is valid.
18. Regarding claim 1, on page 15, the applicant argues the applicant's invention is not limited by the speed of the counter. The applicant does not recite such a limitation in the invention and furthermore, the applicant recites "comprising" which indicates additional components or steps can exist in the apparatus or method. Since the limitation is not recited, the applicant's argument is not relevant to the rejection of the claims.
19. Regarding claim 4, on page 16, the applicant argues Yanagisawa does not determine the edge position movement. Yanagisawa et al discloses "The

comparison pulse generator outputs one phase different comparison pulse after another. Each phase different comparison pulse has width representing the phase different between first and second input signals. The periodic signal generator outputs a periodic signal every time a value obtained by accumulating the widths of the phase difference comparison pulses exceeds a predetermined value." (Abstract, lines 5-12)

20. Regarding claims 2-5,7-10,12-15,17-20 due to the amendments to claims 1,6 and 11, the limitations and references for rejection of these dependent claims have been reconsidered to ensure that there is a possible combination with the references used for the dependent and independent claim. The examiner also recognizes that the applicant argues the references cannot be combined since no specific hint of motivation can be found in the references. The examiner has further included additional explanation for motivation of combination for the dependent claims as well as the independent claims.
21. Regarding claim 2, the rejection is as stated below.
22. Regarding claim 5, the rejection is as stated below.
23. Regarding claims 6 and 11, please refer to the rebuttal of claim 1 as per the applicants argument that the "same issues have been discussed in detail above with respect to claim 1." Also, the rejection has been modified to include additional explanation indicating the motivation for combination between Yanagisawa et al, Kelkar et al and Sunter et al.
24. Regarding claim 7, the rejection is as stated in claim 2.

25. Regarding claim 9, the rejection is as stated in claim 4 along with the rebuttal of claim 4.
26. Regarding claim 10, the rejection is as stated in claim 5.
27. Regarding claim 12, the rejection is as stated in claim 2.
28. Regarding claim 14, the rejection is as stated in claim 4 along with the rebuttal of claim 4.
29. Regarding claim 15, the rejection is as stated in claim 5.
30. Regarding claim 16, please refer to the rebuttal of claims 1,6 and 11 as per the applicant's arguments that the "same issues have been discussed in det ail above with respect to the rejections of claims 1, 6 and 11 and those arguments are equally applicable to the rejection of claim 16." (page 19)
31. Regarding claims 17,the rejection is as stated for claim 12.
32. Regarding Claim 19, the rejection is as stated for claim 4.
33. Regarding claim 20, the rejection is as stated for claim 15.
34. Regarding claim 3, the objection is as stated below.
35. Regarding claims 8,13,18, the rejection is as stated below and as stated for claim 3.

Drawings

36. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. **Since the drawings have no written labels or worded descriptions have been provided in the drawings for any of the components, the examiner cannot determine what components or**

whether any of the components are shown. Therefore, all components must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

37. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

38. **Claims 1,2,3,4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982).

    a. **Claim 1**, Kelkar et al discloses an inputting signal to generate signal transition locations (Fig. 5, labels 84 and 83), latching or sorting the transition location

using a sampling clock signal (Col. 3, lines 42-44), converting the signal transition to a delay value (Col. 3, lines 45-53). Although Kelkar et al does not disclose converting the delay value to an edge position and detecting a value of the edge position, Yanagisawa et al discloses an edge detector converts the first and second signal into first and second timing signals, a comparison pulse generator that outputs the phase difference or delay value of the first and second timing signals. (Fig. 7, labels 107 and 103) It would be obvious to one skilled in the art to combine Kelkar et al's invention with Yanagisawa et al provide a jitter detector for making the jitter between the signals easily detectable by using an edge detector and a comparison pulse generator. (Abstract of Yanagisawa et al, specifically lines 1-3 for motivation and the rest for description of how Yanagisawa's invention) Although Kelkar et al and Yanagisawa et al fails to disclose a data signal, in Kelkar's background, Kelkar et al discloses a "data timing jitter within a digital communication link for monitoring digitally transmitted signals at a receiving point", which inherently discloses a data signal is being monitored, since the system monitors "digitally transmitted signals". (Col. 1, lines 64-67 and Col. 2, lines 1-12) It would be obvious to one skilled in the art to replace the clock signal with a data signal into Kelkar et al's invention based on design choice and to eliminate jitter from the received data so to effectively determine the transmitted data.

b. **Claim 2**, Kelkar et al discloses a PLL for determining the error, which comprises a loop filter (Fig. 5, label 86) prior to capturing the value of the edge. (Fig. 4, label 66)

c. **Claim 3**, Yanagisawa et al and Kelkar et al both disclose a system detecting jitter within an input signal. Although neither Yanagisawa et al and Kelkar et al does not explicitly disclose a dither unit for inserting jitter during a test cycle, since the inputted signal already have jitter when inputted in the prior arts disclosed system, the process of inserting jitter into a signal would inherently have been performed prior to being inputted into the disclosed system. Thus, a dither unit would inherently be included into the disclosed systems of the prior arts inventions.

a. **Claim 4**, Yanagisawa et al discloses a comparator comparing the phase different or edge movement exceeding a predetermined value. (Abstract, lines 5-12)

39. **Claims 6-9, 11-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982) and further in view of Sunter et al. (US Application No.: 20050069031).

a. **Claim 6** inherits all the limitations of Claim 1. Although neither Kelkar et al and Yanagisawa et al discloses a peak-to-peak detection and output, Sunter et al discloses an analysis circuitry measuring and outputting the peak-to-peak value of the latched output data signal. (Fig. 3, label 22) It would be obvious to one

skilled in the art to include an analysis circuitry to provide a "simpler, lower cost technique that accurately measures jitter." (Page 2, paragraph [0015]) It would be obvious to one skilled in the art to combine Sunter et al with Kelkar et al and Yanagisawa et al so to determine the error of the output of the PLL, which comprises either an edge detector, phase detector or some error detector detecting the error between two clock signals or one data signal and a clock signal so to accurately correct such an error and provide as disclosed by Sunter et al "simpler, lower cost technique that accurately measures jitter".

b. **Claim 7** inherits all the limitations of claim 2.

c. **Claim 8** inherits all the limitations of claim 3.

d. **Claim 9** inherits all the limitations of claim 4.

e. **Claim 11**, Kelkar et al discloses a tapped delay line (Fig. 2, labels 33, 35, 37, 39), a sampling clock or a measured clock (Fig. 2, label 26), a sample register for latching the signal transitions. (Fig. 2, labels 36, 38, 40, 42) Although Kelkar et al does not teach a priority encoder, and converter, Yanagisawa et al discloses an encoder in the form of a comparator detecting the phase difference or delay value and a converter in the form of a periodic signal generator outputting a signal for each width or delay value or phase difference. (Fig. 1, labels 103, 104) It would be obvious to one skilled in the art to combine Kelkar et al's invention with Yanagisawa et al to produce multiple delays of the input signal to make the jitter between the signals easily detectable. (Abstract of Yanagisawa et al, lines 2-3) Although neither Kelkar et al nor Yanagisawa et al

discloses a peak-to-peak detector, Sunter et al discloses an analysis circuit that calculates the peak-to-peak value of the latched signal. (Fig. 6A, label 22) It would be obvious to one skilled in the art to include an analysis circuitry to provide a "simpler, lower cost technique that accurately measures jitter." (Page 2, paragraph [0015]) It would be obvious to one skilled in the art to combine Sunter et al with Kelkar et al and Yanagisawa et al so to determine the error of the output of the PLL, which comprises either an edge detector, phase detector or some error detector detecting the error between two clock signals or one data signal and a clock signal so to accurately correct such an error and provide as disclosed by Sunter et al "simpler, lower cost technique that accurately measures jitter".

f. **Claim 12** inherits all the limitations of claim 2, but claim 2 does not recite filtering prior to peak to peak detecting the edge positions. Sunter et al disclose filtering prior to analyzing the circuit (Fig. 6b, label filter), wherein the analysis circuit comprises determining the peak-to-peak value of the edge positions. (paragraph [0022], lines 1-2)

g. **Claim 13** inherits all the limitations of claim 3.

h. **Claim 14** inherits all the limitations of claim 4.

40. **Claims 16-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982) further in view of Sunter et al. (US Application No.: 20050069031) and

further in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial".

a. **Claim 16** inherits all the limitations of claim 11. Although a field programmable gate array carry chain (FPGA carry chain) is not disclosed by Kelkar et al, Yanagisawa et al and Sunter et al, based on the tutorial provided by IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial", an FPGA is a programmable array of flip-flops or logic gates. Kelkar et al discloses a variable delay line, which is equivalent to an FPGA. (Fig. 5, label 83) It would be obvious to one skilled in the art to provide an FPGA carry chain comprised of an interchanging or programmable delay line to provide a more robust, dynamic array of logics to decrease cost and provide very high pin-to-pin speed performance. (Definitions: page 43 under Terminology, pg 43, Col. 3, line 4 and pg 44, Col. 1, lines 1-2) It would be obvious to one skilled in the art to incorporate an FPGA into Kelkar et al, Yanagisawa et al, and Sunter et al's invention to substitute the delay line as disclosed by Kelkar et al so to provide a more robust, dynamic array of logics to decrease cost and provide very high pin-to-pin speed performance. (Definitions: page 43 under Terminology, pg 43, Col. 3, line 4 and pg 44, Col. 1, lines 1-2)

b. **Claim 17** inherits all the limitations of claim 12.

c. **Claim 18** inherits all the limitations of claim 3.

d. **Claim 19** inherits all the limitations of claim 4.

41. **Claim 5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982) , and further in view of Jungerman et al (US Publication No.: 20040146097).

    a. **Claim 5**, Although Kelkar et al and Yanagisawa et al does not disclose calculating the root mean square (RMS) of the edge position, Jungerman et al discloses a method of detecting jitter at an edge (Abstract, lines 1-5) comprising calculating the RMS value of the slope of the designated edge corresponding to the random component of the jitter. (page 1, paragraph [0005] and Fig. 2) It would be obvious to one skilled in the art to measure the RMS value at the position of the edge as taught by Jungerman et al determine the periodic component of the jitter so to eliminate affects caused by jitter. (paragraph [0002]) It would be obvious to one skilled in the art to combine Jungerman et al to Kelkar et al and Yanagisawa et al's invention to determine jitter as both invention performs such a task (Jungerman et al, paragraph [0005], Kelkar et al, Abstract, and Yanagisawa et al, Abstract, lines 1-3) by detecting the phase error or edge error or transition edge as disclosed by the three references. (Kelkar et al, Abstract, and edge sorting circuit, Fig. 1, label 12, Yanagisawa et al, Abstract, and Jungerman et al, paragraph [0005])

2. **Claims 10,15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.:

6528982), further in view of Sunter et al. (US Application No.: 20050069031) and further in view of Jungerman et al (US Publication No.: 20040146097).

a. **Claim 10** inherits all the limitations of claim 5.

b. **Claim 15** inherits all the limitations of claim 5, but claim 5 does not recite performing root mean square is connected for analyzing the edge position output. Jungerman et al disclose using the edge, which has a position (Fig. 3a, label a1 and Fig. 2, label 22) to provide the root mean square value. (Abstract)

2. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelkar et al (US Patent No.: 5663991) in view of Yanagisawa et al. (US Patent No.: 6528982), further in view of Sunter et al (US Publication No.: 20050069031), further in view of IEEE Design and Test of Computers, "FPGA and CPLD Architectures: A Tutorial" and further in view of Jungerman et al (US Publication No.: 20040146097)..

a. **Claim 20** inherits all the limitations of claim 15.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

4. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong

DAC HA
PRIMARY EXAMINER